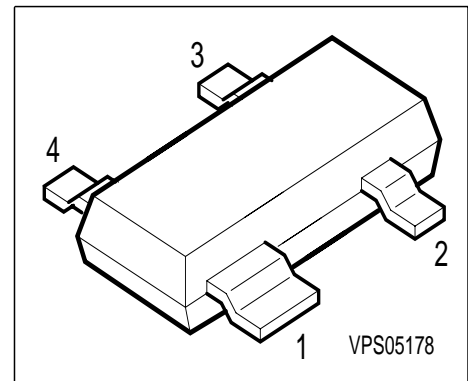


Silicon N-Channel MOSFET Tetrode

Preliminary data

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 5V



ESD: Electrostatic discharge sensitive device, observe handling precaution

Type	Marking	Ordering Code	Pin Configuration				Package
BF 2030	NEs	Q62702-F1773	1 = S	2 = D	3 = G2	4 = G1	SOT-143

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	14	V
Continuous drain current	I_D	40	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	7	V
Total power dissipation, $T_S = 76\text{ °C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... +150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point	R_{thchs}	≤ 370	K/W
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Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage $I_D = 650 \mu\text{A}$, $-V_{G1S} = 4 \text{ V}$, $-V_{G2S} = 4 \text{ V}$	$V_{(BR)DS}$	-	12	-	V
Gate 1 - source breakdown voltage $+I_{G1S} = 10 \text{ mA}$, $V_{G2S} = 0 \text{ V}$, $V_{DS} = 0 \text{ V}$	$+V_{(BR)G1SS}$	-	8.5	-	
Gate 2 - source breakdown voltage $\pm I_{G2S} = 10 \text{ mA}$, $V_{G1S} = V_{DS} = 0$	$+V_{(BR)G2SS}$	-	8.5	-	V
Gate 1 source current $V_{G1S} = 6 \text{ V}$, $V_{G2S} = 0 \text{ V}$	$+I_{G1SS}$	-	-	50	nA
Gate 2 source leakage current $V_{G2S} = 8 \text{ V}$, $V_{G1S} = 0 \text{ V}$, $V_{DS} = 0 \text{ V}$	$+I_{G2SS}$	-	-	50	
Drain current $V_{DS} = 5 \text{ V}$, $V_{G1S} = 0$, $V_{G2S} = 4.5 \text{ V}$	I_{DSS}	-	-	-	μA
Drain-source current $V_{DS} = 5 \text{ V}$, $V_{G2S} = 4.5$, $R_{G1} = 20 \text{ k}\Omega$	I_{DSX}	-	12	-	mA
Gate 2-source pinch-off voltage $V_{DS} = 5 \text{ V}$, $I_D = 100 \mu\text{A}$	$V_{G2S(p)}$	0.3	0.8	-	V
Gate 1-source pinch-off voltage $V_{DS} = 5 \text{ V}$, $V_{G2S} = 4 \text{ V}$, $I_D = 200 \mu\text{A}$	$V_{G1S(p)}$	0.3	0.7	-	
AC characteristics					
Forward transconductance $V_{DS} = 5 \text{ V}$, $I_D = 10 \text{ mA}$, $V_{G2S} = 4 \text{ V}$, $f = 1 \text{ kHz}$	g_{fs}	-	31	-	mS
Gate 1 input capacitance $V_{DS} = 5 \text{ V}$, $I_D = 10 \text{ mA}$, $V_{G2S} = 4 \text{ V}$, $f = 1 \text{ MHz}$	C_{g1ss}	-	3	-	pF
Output capacitance $V_{DS} = 5 \text{ V}$, $I_D = 10 \text{ mA}$, $V_{G2S} = 4 \text{ V}$, $f = 1 \text{ MHz}$	C_{dss}	-	2.1	-	
Noise figure $V_{DS} = 5 \text{ V}$, $I_D = 10 \text{ mA}$, $f = 800 \text{ MHz}$	F	-	2	-	dB